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Listing of Claims:

1. (Original) A transconductance amplifier with multi-emitter structure for balancing current of a multi-phase regulator, comprising:

a plurality of transistors, each having first and second current terminals and a current control terminal receiving a corresponding one of a plurality of sense voltages, each sense voltage indicative of output inductor current of a corresponding phase of the multi-phase regulator;

a bias current device coupled to the first current terminals of each of said plurality of transistors;

a plurality of current mirrors, each having an input coupled to a second current terminal of a corresponding one of said plurality of transistors and an output coupled to a corresponding one of a plurality of correction nodes; and

a plurality of current sources, each coupled to a corresponding one of said plurality of correction nodes.

2. (Original) The transconductance amplifier of claim 1, wherein said plurality of transistors comprise N transistors, wherein said bias current device develops a current IB, and wherein each of said plurality of current sources develops a current IB/N.

3. (Original) The transconductance amplifier of claim 2, wherein said bias current device comprises:

a current source sourcing a current IB;

a diode-coupled first device coupled to said current source; and

a second device having an input coupled to said diode-coupled device in a 1:1 current mirror configuration and an output coupled to said first current terminal of each of said plurality of transistors.

4. (Original) The transconductance amplifier of claim 3, wherein each of said plurality of current mirrors comprises a third device having an input coupled to said first device in a 1:N current mirror configuration and an output coupled to a corresponding one of said plurality of correction nodes.

5. (Original) The transconductance amplifier of claim 4, wherein said first, second and third devices each comprise NMOS transistors.

6. (Original) The transconductance amplifier of claim 1, wherein each of said plurality of transistors comprises a bipolar transistor.

7. (Original) The transconductance amplifier of claim 6, wherein said first and second terminals of said plurality of transistors comprise emitters and collectors, respectively.

8. (Original) The transconductance amplifier of claim 1, wherein each of said plurality of sense voltages is based on a corresponding voltage of a DCR of a corresponding one of a plurality of output inductors.

9. (Original) The transconductance amplifier of claim 1, further comprising a plurality of input amplifier filter stages, each receiving a corresponding one of said plurality of sense voltages and providing a corresponding one of a plurality of buffered voltages provided to said plurality of transistors.

10. (Original) An N-phase regulator, comprising:

N output circuits for each of N phases;

N output current sensing circuits, each sensing output current of a corresponding one of said N output circuits and providing a corresponding one of N sense voltages;

a transconductance amplifier with multi-emitter structure, comprising:

N transistors, each having first and second current terminals and a control terminal receiving a corresponding one of said N sense voltages;

a bias current device coupled to said first current terminals of each of said N transistors;

N current mirrors, each having an input coupled to a second terminal of a corresponding one of said N transistors and an output coupled to a corresponding one of N correction nodes; and

N current sources, each coupled to a corresponding one of said N correction nodes; and

a power circuit having N inputs each coupled to a corresponding one of said N correction nodes and N outputs each providing a PWM signal with corrected duty cycle to a corresponding one of said N output circuits.

11. (Original) The regulator of claim 10, wherein said bias current device develops a current IB, and wherein each of said N current sources sinks a current IB/N.

12. (Original) The regulator of claim 10, wherein each of said N sense voltages is based on a corresponding voltage of a DCR of a corresponding one of N output inductors of said N output circuits.

13. (Original) The regulator of claim 10, wherein said power circuit comprises an N-channel modulator block that adjusts duty cycle of each of N PWM signals based on a corresponding one of said N correction currents.

14. (Original) A method of balancing current in an N-phase regulator, comprising:

sensing output current for each of the N phases and providing corresponding N feedback sense voltages;

biasing N transistors with a total bias current of IB;

applying each of the N feedback sense voltages to a control input of a corresponding one of the N transistors to develop N sense currents;

mirroring each of the N sense currents into a corresponding one of N correction nodes;

sourcing a current of IB/N relative to each of the N correction nodes to provide N correction currents; and

adjusting current of each of the N phases based on a corresponding one of the N correction currents.

15. (Original) The method of claim 14, wherein said sensing output current comprises sensing voltage across the DCR of an output inductor.

16. (Original) The method of claim 14, wherein said biasing N transistors comprises sourcing a current IB relative to common-coupled emitters of the N transistors.

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17. (Original) The method of claim 14, wherein said sourcing a current of IB/N relative to each of the N correction nodes comprises drawing a current of IB/N from each of the N correction nodes.

18. (Original) The method of claim 14, wherein said adjusting current of each of the N phases comprises adjusting duty cycle of each of N PWM control signals.